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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/696,104	10/24/00	FT. NAFFZIGER	S 10005465-1

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EXAMINER	
NGUYEN,	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/20/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/696,104	FT. NAFFZIGER, SAMUEL D.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2000* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "an inverse of a dynamic logic evaluate clock" in claim 1, claim 5 and claim 15, the "said delay comprised of a plurality of inverters" in claim 2, claim 8 and claim 12, the "a clock that is the inverse of a second clock" in claim 9 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Objections

2. Claim 14 is objected to because of the following informalities: "a delay element" on line 2 should be changed to --said delay element--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1-12, 15, and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, the recitation "wherein said delay input and said clock input connect to an inverse of a dynamic logic evaluate clock" appears to be misdescriptive because it is inconsistent with what is disclosed and shown in the drawing because Figure 1 of the drawing

does not show that the delay input and the clock input connect to an inverse of a dynamic logic evaluate clock. Note that the same problem also exists in claims 5, 9 and 15

Claims 2-4, 6-8, 10-12, and 16 are indefinite because they depend on claims 1, 5, 9, and 15, respectively.

Claim 11 is also indefinite because the recitation "the interface of claim 11" is not clear because it is not understood how claim 11 also depends on claim 11. It appears that claim 11 depends on claim 10.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2, 5, 7, 8, 9, 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin et al. (USP 5,734,841).

Insofar as understood in claims 1, 5, and 13, Figure 2 of the Shin et al. reference discloses a circuit which includes: a delay (INT1-INT8) having a delay input and delay output; and a latch (INT10 and FF inside circuit 10) having a clock input (cp), an enabled input (cdn), a data input (d) and a data output (q) and wherein the delay input and the clock input connected to a clock signal (CLK) and the delay output connects to the enable input (cdn).

With respect to claims 2 and 8, it is seen in Figure 2 that the delay includes of a plurality of inverters (INT1-INT8).

Insofar as understood in claim 7, it is seen in Figure 2 that the delay version of the clock is generated by supplying a delay element with the clock (CLK).

Insofar as understood in claim 9, Figure 2 of the Shin et al. reference discloses a circuit which includes: a clock (CLK); a delay element (INT1-INT8) that generates a delayed clock (output of INT8); and a latch (INT10 and FF inside circuit 10) having a clock input (cp) that receives the clock, an enabled input (cdn) that receives the delayed clock, a data input (d) and a data output (q). Note that the recitation "that interfaces to static logic" and the recitation "that interfaces to dynamic logic" are intended use.

7. Claims 1, 3, 5, 6, 7, 9, 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Pathak et al. (USP 4,879,481).

Insofar as understood in claims 1, 5, and 13, Figure 2 of the Pathak et al. reference discloses a circuit which includes: a delay (73) having a delay input and delay output; and a latch (74-77) having a clock input (gate of 75), an enabled input (gate of 74), a data input (IN) and a data output (OUT) and wherein the delay input and the clock input connected to a clock signal (output of 72) and the delay output connects to the enable input (gate of 74).

With respect to claims 3 and 6, it is seen in the Pathak et al. reference that the latch (74-77) in Figure 2 is a transparent latch.

Insofar as understood in claim 7, it is seen in Figure 2 that the delay version of the clock is generated by supplying a delay element with the clock.

Insofar as understood in claim 9, Figure 2 of the Shin et al. reference discloses a circuit which includes: a clock (output of 72); a delay element (73) that generates a delayed clock (output of 73); and a latch (74-77) having a clock input (gate of 75) that receives the clock, an

enabled input (gate of 74) that receives the delayed clock, a data input (IN) and a data output (OUT). Note that the recitation "that interfaces to static logic" and the recitation "that interfaces to dynamic logic" are intended use.

With respect to claim 14, it is seen in the operation of the circuit in Figure 2 of the Pathak et al. reference that the latch (74-77) is open until the clock input (output of 72) falls and the latch remains closed until the delay element (73) delays after the clock input (output of 72) rises.

Insofar as understood in claim 15, Figure 2 of the Pathak et al. reference shows that the clock input (gate of 75) is coupled to a clock (output of 72).

With respect to claim 16, it is seen in Figure 2 of the Pathak et al. reference that the delay element includes at least one inverter (73).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 4, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pathak et al. (USP 4,879,481) in view of Baco (USP 5,968,180).

With respect to claims 2, 4 and 8, Figure 2 of the Pathak et al. discloses a circuit which meets all the limitations of this claim as discussed in the above 102 rejection. The Pathak et al. reference does not disclose that the delay element includes a plurality of inverters. However, Figure 4 of the Baco reference discloses a delay circuit which includes a plurality of inverters (71, 73 ... 77, 79) for achieving an optimal delay period (Col. 6, lines 44-46). Therefore, it

would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the circuit in Figure 2 of the Pathak et al. reference to use a plurality of inverters (e.g., 3 or 5 inverters) for the delay element instead just one inverter (73) to achieve an optimal delay period. It is seen that this modification meets all the limitations of claims 2, 4 and 8.

Allowable Subject Matter

10. Claims 10-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 10 is allowed because none of the prior art of record discloses or suggests a static to dynamic interface which includes all the limitations of this claim. In particular, the prior art of record fails to disclose that the latch of the interface including a first pass gate and a second pass gate with the recited connections and operations set forth in claim 10.

Claims 11 and 12 are allowed because they depend on claim 10.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Long Nguyen whose telephone number is (703) 308-6063. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 308-7722.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

June 6, 2001

L N

Long Nguyen
Art Unit: 2816

Terry D. Cunningham
Primary Examiner